Claims

What is claimed is:

[c1] A method of visualizing events within a microprocessor comprising:

receiving internal state information representative of events occurring in the microprocessor; and

graphically displaying an execution behavior of the instructions on the microprocessor based on the internal state information.

[c2] The method of visualizing events within a microprocessor of claim 1, further comprising:

receiving a set of instructions;

executing the set of instructions on the microprocessor; and

monitoring the internal state information representative of events occurring in the microprocessor.

[c3] The method of visualizing events within a microprocessor of claim 1, further comprising:

receiving a design for the microprocessor;

receiving a set of instructions;

simulating operation of the microprocessor for the set of instructions in accordance with the design; and

generating the internal state information representative of events occurring in the microprocessor from the simulation.

[c4] The method of visualizing events within a microprocessor of claim 1, further comprising:

receiving a set of instructions;

exporting the set of instructions to a microprocessor simulator that simulates operation of the microprocessor for the set of instructions and generates internal state information representative of events occurring within the microprocessor; and

receiving the internal state information representative of events occurring in the microprocessor from the microprocessor simulator.

[c5] The method of visualizing events within a microprocessor of claim 3, further comprising:

displaying a selected number of types of execution behavior of the set of instructions on the microprocessor.

[c6] The method of visualizing events within a microprocessor of claim 3, further comprising:

displaying the execution behavior of the set of instructions on the microprocessor occurring during a selected number of time periods.

[c7] The method of visualizing events within a microprocessor of claim 3, further comprising:

creating a log of the execution behavior of the set of instructions on the microprocessor.

[c8] The method of visualizing events within a microprocessor of claim 1, further comprising:

graphically displaying selectable instructions;

creating a set of instructions from selected instructions;

simulating operation of the set of instructions on the microprocessor; and

generating the internal state information representative of events occurring in the microprocessor from the simulation.

[c9] The method of visualizing events within a microprocessor of claim 4 further comprising:

converting the received internal state information representative of events occurring in the microprocessor into a form usable by a display module that graphically displays execution behavior based on internal state information; and

sending the converted internal state information to the display module for graphical display of the execution behavior based on the converted internal state information.

[c10] The method of visualizing events within a microprocessor of claim 2, wherein the graphical display represents a flow of the instructions through an internal pipeline in the microprocessor.

[c11] A software tool for visualizing events within a microprocessor, the software tool comprising:

a program stored on computer-readable media for

receiving internal state information representative of events occurring in the microprocessor; and

graphically displaying an execution behavior of the set of instructions on the microprocessor based on the internal state information.

[c12] The software tool of visualizing events within a microprocessor of claim 11, further comprising:

a program stored on computer-readable media for

receiving a set of instructions;

executing the set of instructions on the microprocessor; and

monitoring the internal state information representative of events occurring in the microprocessor.

[c13] The software tool for visualizing events within a microprocessor of claim 11, further comprising:

a program stored on computer-readable media for

receiving a design for the microprocessor;

receiving a set of instructions;

simulating operation of the microprocessor for the set of instructions from the design; and

generating the internal state information representative of events occurring in the microprocessor from the simulation.

[c14] A system for visualizing events within a microprocessor, the system comprising:

an interface module that receives a set of instructions;

a microprocessor simulator that simulates operation of the microprocessor for the set of instructions and generates internal state information representative of events occurring within the microprocessor; and

a display module that graphically displays an execution behavior of the set of instructions on the microprocessor based on internal state information;

wherein the interface module exports the received set of instructions to the microprocessor simulator, imports the internal state information representative of events occurring in the microprocessor from the microprocessor simulator, and communicates the internal state information to the display module.

[c15] The system for visualizing events within a microprocessor of claim 14, wherein the display module displays a selected number of types of execution behavior of the set of instructions on the microprocessor.

[c16] The system for visualizing events within a microprocessor of claim 14, wherein the display module displays the execution behavior of the set of instructions on the microprocessor occurring during a selected number of time periods.

[c17] The system for visualizing events within a microprocessor of claim 14, the interface module comprising:

a conversion module that converts the set of instructions received into a form understandable by the microprocessor simulator and converts the internal state information into a form understandable by the display module.

[c18] A tool for visualizing events within a microprocessor comprising:

means receiving internal state information representative of events occurring in the microprocessor; and

means for graphically displaying an execution behavior of the instructions on the microprocessor based on the internal state information.

[c19] The tool for visualizing events within a microprocessor of claim 18, further comprising:

means for simulating operation of a microprocessor for a set of instructions; and

means for generating internal state information from the simulation.

[c20] The tool for visualizing events within a microprocessor of claim 18, further comprising:

means for exporting a set of instructions to a simulator in a understandable form;

means for importing results from the simulator; and

means for converting the results into internal state information representative of events occurring in the microprocessor.